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*FORM PTO-1390 OFFICE (REV 11-2000)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK	ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371		449122010300
		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/937371 Not yet assigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/01762	March 1, 2000	March 23, 1999

TITLE OF INVENTION

CIRCUIT ARRANGEMENT FOR PROCESSING AN ATM CELL HEADER

APPLICANT(S) FOR DO/EO/US

Elena GRIGORE et al.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information: 1. International Search Report 2. IPER 3. Application Data Sheet 4. Return receipt postcard.

OIPE JC152 SEP 2 4 2001 PATENT & TRADEMARK OFFICE

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on September 24, 2001.

Melissa Garton

dc-280669

U.S. APPLICATION NO. (if known, see 37 CFR 1.5) Not yet assigned 09/937371	INTERNATIONAL APPLICATION NO. PCT/EP00/01762	ATTORNEY'S DOCKET NUMBER: 449122010300

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO $1,000.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $860.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provision of PCT Article 33(1)-(4) $690.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

	CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$0	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	9 - 20 =	0	x $18.00	$0	
Independent claims	1 - 3 =	0	x $80.00	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$270.00	
TOTAL OF ABOVE CALCULATIONS =				$860.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.				$0	
SUBTOTAL =				$1130.00	
☐ Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$0	
TOTAL NATIONAL FEE =				$1130.00	
☐ Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property** +				$40.00	
TOTAL FEES ENCLOSED =				$1170.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ Please charge my **Deposit Account No. 03-1952** in the amount of $1170.00 to cover the above fees. Please reference 449122010300. A duplicate copy of this sheet is enclosed.

b. ☒ The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952**. Please reference 449122010300. A duplicate copy of this sheet is enclosed.

c. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kevin R. Spivak
Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
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SIGNATURE

Kevin R. Spivak
Registration No. 43,148

°FORM PTO-1390 (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

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CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on September 24, 2001.

Melissa Garton

dc-280669

Description

Circuit arrangement for processing an ATM cell header.

The invention relates to a circuit arrangement according to the precharacterizing clause of patent claim 1.

In contemporary information processing systems, information is transmitted in packets, such as in ATM cells or IP packets. An ATM cell comprises a cell header having a length of 5 bytes and an information part having a length of 48 bytes. The information part is used to transmit the actual user information, while the cell header stores an address and other cell information. A total of 4 bytes need to be reserved for the latter. The fifth byte is then used to concomitantly transmit a check information item which can be used to ascertain and, if appropriate, correct any erroneous transmission of the cell header.

This check information item can be regarded as part of the cell header and is referred to as the HEC field (HEC = Header Error Control). This field having a length of 1 byte stores a complex checksum relating to the address contained in the cell header.

Generally, the cell header needs to be generated and placed in front of the information part before the transmission operation in the transmitting device. At the reception end, the cell header is received in the receiving device, and the user information transmitted in the information part is supplied to the device denoted by the address. For this purpose, the ATM cell header having the check information item thus needs to be generated in the transmitting device and evaluated in the receiving device, with generation and evaluation of the check information item being standardized. If,

by way of example, transmission errors are ascertained, they can be corrected again - albeit to a limited extent.

The check information item is generated and evaluated using specially designed interface circuits referred to below as header processing circuits, or processing circuits for short. The transmitting device thus uses the processing circuit arranged therein to generate the check information item, and the receiving device uses the processing circuit arranged therein to evaluate it. The processing circuit arranged at the transmission end thus has a generation function, while the processing circuit arranged at the reception end has an evaluation and correction function. Since transmission takes place bidirectionally, each transmitting and receiving device has both types of processing circuits.

During the transmission operation, the ATM cells are generally inserted into a specific transmission format (e.g. SDH format, Synchronous Digital Hierarchy), and are removed from it again at standardized interfaces. In the case of the SDH transmission format, these are STM interfaces.

A simple form of such an interface is the STM-1 interface. More complex interfaces are in the form of N*STM-1 interfaces. In the case of the nonconcatenated mode (N > 1), in which the ATM cells from a plurality of sources are transmitted via just one path, this means that the processing circuits need to be used a plurality of times. By way of example, when transmitting 4*STM-1 signals, such signals are converted to one STM-4 signal. This signal is then routed via the path in question and is converted into 4*STM-1 signals again at the reception end. This means that 4 processing circuits need to be arranged for each STM-4 channel, e.g. at the transmission end. The same applies for the processing circuits arranged in the receiving device. In the case of higher-order

interfaces (e.g. STM-16 etc.), the multiplicity of processing circuits thus rises drastically. However, this results not

only in problems with the complexity of the overall transmission system (e.g. increased susceptibility to error), especially since each processing circuit itself actually has an increased level of complexity, but also in problems with an increased power consumption for the chips in the interfaces, and with associated heating. In addition, this entails an increased cost requirement.

The invention is based on the object of specifying a circuit arrangement which reduces the multiplicity of processing circuits to a practical level.

The invention is achieved, on the basis of the precharacterizing clause of patent claim 1, by the features specified in the characterizing part. The advantage of the invention can be seen in that the processing circuits have further devices connected to them such that the processing circuits need to be provided just once for a plurality of channels. This means, for example in the case of an STM-4 interface having 4 channels, that just one processing circuit needs to be provided instead of 4 processing circuits in the prior art. This obviates 3 complex processing circuits in the case of STM-4nc signals.

Advantageous developments of the invention are specified in the subclaims.

The invention is explained in more detail below using an exemplary embodiment shown in figures, in which:

Figure 1 shows the reception-end transmission of STM-4 signals in nonconcatenated mode

Figure 2 shows the inventive circuit arrangement.

Figure 1 shows the transmission of STM-4 signals in nonconcatenated mode. In this case, the packets are in the form of ATM cells and are embedded in STM-1 signal. The 4*STM-1 signals are combined in one STM-4 signal. At the reception end, the STM-4 signal needs to be restored to the respective 4*STM-1 signals again.

The way in which the circuit arrangement works will now be explained in more detail below on the basis of figure 2. In this figure, ATM cells are supplied via an SDH interface. By way of example, STM-4 signals need to be transmitted. In the text below, these are supplied as 4 STM-1 signals via channels $CH_0 \ldots CH_3$. In addition, it is assumed that ATM cells are supplied to a receiving device. In this case, the processing circuit is designed such that the cell header of the incoming ATM cell is checked for correct transmission. The processing circuit thus has an evaluation and correction function and, as such, is known and is not the subject matter of the invention, which is why no further description is given of a detailed manner of operation.

The ATM cells are thus first supplied via the four channels $CH_0 \ldots CH_3$ to a separating device HPS (Header Payload Separation). There, the ATM cell header is separated from the information part. The user information (payload) is written to a cell memory SP arranged downstream, with a counting device WAC (Write Address Counter) generating and storing the information about where the information part of each ATM cell is stored. This information is necessary in this respect because, later, the processed ATM cell header is placed in front of the information part again and the ATM cell is forwarded.

The cell headers associated with the ATM cells arriving in the separating device HPS are now stored in an FIFO memory device HEAD in the order of arrival.

It may be assumed, by way of example, that an ATM cell in the channel CH_0 arrives first in the separating device HPS. Consequently, the separated ATM cell header is written to the first location in the FIFO memory device HEAD. Next, an ATM cell in the channel CH_2 will arrive in the separating device HPS. The associated ATM cell header is stored in the FIFO memory device HEAD directly behind the already stored cell header of the ATM cell from the channel CH_0. In the same way, the ATM cell headers of the ATM cells associated with the channels CH_1, CH_3 are stored in the FIFO memory device HEAD. Each ATM cell header requires 4 bytes of memory space.

With the ATM cell header, the check information item HEC having a length of 1 byte is also separated from the information part and is stored in another FIFO memory device HECC. Storage takes place in the same order as storage of the cell headers in the FIFO memory device HEAD. Consequently, the check information HEC of the ATM cell which has arrived in the channel CH_0 is likewise stored at the first location in the FIFO memory device HECC.

Finally, a third FIFO memory device CI (Channel Identifier) is also arranged. This stores information about which channel has the information stored in the FIFO memory devices HEAD and HECC associated with it. This is necessary to this extent because it is not possible to tell from the information stored there which ATM cell from which channel is its origin. In the present exemplary embodiment, the information stored at the first location in the FIFO memory device CI signals that the information stored in the FIFO memory devices HEAD and HECC is associated with the channel CH_0.

The cell header stored in the first field of the FIFO memory device HEAD, which cell header is meant to be associated with the channel CH_0 on the basis of the present exemplary embodiment, is now supplied

to the processing circuit BS as an input parameter. At the same time as this, the check information item HEC is supplied as a second input parameter.

The ATM cell header and the check information item HEC are now logically combined in the processing circuit BS and are examined to determine whether the cell header has been transmitted correctly. If this is the case, the ATM cell header is stored unaltered in devices downstream. These are in the form of registers $R_0 \ldots R_3$ for individual channels. In this case, the ATM cell header for channel CH_0 is stored in register R_0, the ATM cell header for channel CH_1 is stored in register R_1 etc. In this context, the information stored in the FIFO memory device CI is taken as the criterion for which of the registers $R_0 \ldots R_3$ needs to store the ATM cell header. On the basis of the present exemplary embodiment, the ATM cell header being checked by the processing circuit BS is thus stored in register R_0. Once this processing operation is complete, the information stored in the FIFO memory devices HEAD, HCC is received by the processing circuit BS and is processed in the same way.

The registers $R_0 \ldots R_3$ for individual channels also store other information. Thus, in addition to the ATM cell header, they store the associated check information item HEC and a header information item. The latter bears a total of 3 information items. First, it stores whether or not the ATM cell header has been transmitted correctly. Secondly, it also bears an information item regarding whether or not the ATM cell header can be corrected if the latter situation applies. This last information item is a fundamental aspect for bringing together the information part and the ATM cell header. If the ATM cell header cannot be corrected, the whole ATM cell is rejected.

The information part of the ATM cells has - as already mentioned - been stored in a cell memory SP under the control of the counting device WAC after leaving the separating device HPS. This memory thus stores the information parts of the separated ATM cells. They are stored by virtue of bytes 6 to 53 of the information part being stored first. In addition, bytes 1 to 5 in the cell memory SP are reserved directly in front of the information part for the purpose of later storage of the (possibly corrected) cell header and of the check information item HEC.

Under the control of the counting device WAC, the cell headers are now stored directly in front of the user information (payload). These are, first, bytes 1...4, which specify an address. In addition, the check information item HEC is stored at byte 5. If the cell header has been incorrigibly corrupted during the transmission operation, this cell is rejected by enabling the memory area which currently stores the user information associated with this cell header in order to overwrite this memory area with the information part of the next cell. The now complete ATM cells are then read from the cell memory SP and are supplied to further devices.

In the prior art, the cell header is furthermore processed first, and only then is the information part added to the processed cell header. This has the drawback that the information part needs to be added with a delay, because processing the cell header takes much more time than transmitting and storing the information part. In terms of circuitry, this means that delay cycles need to be inserted using special HW devices. The converse procedure proposed in the exemplary embodiment - that is to say first storing the

information part and then adding the processed cell header - obviates these delay cycles with the associated special HW devices.

In the present exemplary embodiment, it has been assumed that the processing circuit BS has an evaluation and correction function. However, this does not signify any restriction, since the processing circuit BS can likewise have a generation function and, in the same way, can have the FIFO memory devices HEAD, HECC, CI and the registers connected to it as in figure 2. In this case, the header information item stored in the registers $R_0 \ldots R_3$ for individual channels is omitted, however.

Patent claims

1. A circuit arrangement for processing a packet header, having a transmission device which supplies packets in a plurality of channels ($CH_0 \ldots CH_3$) to a further transmission device, and having
at least one processing circuit (BS) which is respectively arranged in one of the transmission devices and which processes the packet header of each packet in accordance with a check information item (HEC),
characterized
in that at least one memory device (HEAD, HCC, CI) is provided which stores information relating to the packet header in the order of arrival of the packets routed via the plurality of channels ($CH_0 \ldots CH_3$), and
in that the processing circuit (BS) receives this information, processes it and forwards the packets in accordance with the processing result.

2. The circuit arrangement as claimed in claim 1, characterized
in that the processing circuit (BS) has a generation function which is used to ascertain the check information item (HEC) ascertained using the packet header and to store it in the packet header.

3. The circuit arrangement as claimed in claim 1, characterized
in that the processing circuit (BS) has an evaluation and correction function which is used to logically combine the packet header with the

concomitantly transmitted check information item (HEC) and to correct it, if appropriate, in accordance with the result.

4. The circuit arrangement as claimed in claim 1 or 2,
characterized
in that the information relating to the packet header is an address information item, the check information item (HEC) and a channel-specific information item.

5. A circuit arrangement as claimed in claim 1 to 4, characterized
in that the at least one memory device (HEAD, HCC, CI) is in the form of an FIFO memory device.

6. The circuit arrangement as claimed in one of the preceding claims,
characterized
in that a separating device (HPS) is provided which separates the packets into packet header and information part.

7. The circuit arrangement as claimed in one of the preceding claims,
characterized
in that a control device (WAC) routes information about the assocation of a packet header with the corresponding information part.

8. The circuit arrangement as claimed in one of the preceding claims,
characterized
in that a cell memory (SP) for holding the separate information part of the packets is provided in which memory space for holding the processed packet header is additionally reserved.

9. The circuit arrangement as claimed in one of the preceding claims,
characterized
in that the packets are in the form of ATM cells.

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Schaltungsanordnung zum Bearbeiten eines ATM-Zellenkopfes

Circuit arrangement for processing an ATM cell overhead

deren Beschreibung

the specification of which

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 01.03.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/EP00/01762
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

(check one)
☐ is attached hereto.
☒ was filed on 01.03.2000 as
PCT international application
PCT Application No. PCT/EP00/01762
and was amended on _____
(if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications Priorität beansprucht			Priority Claimed	
99105873.6	EP	23.03.1999	☒	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/EP00/01762 (Application Serial No.) (Anmeldeseriennummer)	01.03.2000 (Filing Date D, M, Y) (Anmeldedatum T, M, J)	anhängig (Status) (patentiert, anhängig, aufgegeben)	pending (Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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German Language Declaration

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